

Attorney's Docket No.: 10559/403001/P10340

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Mark A. Anders et al. Confirmation No.: 7194
Serial No.: 09/895,278 Art Unit : 2814
Filed : June 29, 2001 Examiner : Dana Farahani
Title : DYNAMIC BUS REPEATER WITH IMPROVED NOISE TOLERANCE

Commissioner for Patents
Washington, D.C. 20231

RESPONSE

In response to the action mailed April 10, 2002, please
amend the application as follows:

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In the specification:

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Please replace paragraph [0011] with the following
rewritten paragraph:

A1 --Figure 2 is a circuit diagram of an exemplary dynamic driver 200. The driver includes a domino gate 202 and an inverter 204. In the pre-charge phase, the $\phi 1$ clock signal is LOW. PMOS transistor 206 is turned on, providing a path from Vcc, and NMOS transistor 208 is turned off, closing the path to Vss. This pulls intermediate node 210 HIGH, which is inverted to a LOW signal by the inverter 204. The LOW pre-charge signal

CERTIFICATE OF TRANSMISSION BY FACSIMILE

I hereby certify that this correspondence is being transmitted by facsimile to the Patent and Trademark Office on the date indicated below.

July 10, 2002
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